Registers General Descriptions

* Software Reset Register
  + 0x[C\_BASEADDR + 40]
  + Write only
    - Only allows write of 0x0000\_000A for software reset
* SPI Control Register
  + 0x[C\_BASEADDR + 60]
  + R/W
    - Control register for SPI module functionality including:
      * LSB first transfer format
      * Master transaction inhibit and manual slave select assertion enable
      * FIFO resets
      * Clock phase and clock polarity
      * Master/slave configuration bit
      * SPI system enable
      * Loopback mode enable
* SPI Status Register
  + 0x[C\_BASEADDR + 64]
  + Read only
    - Status register for SPI module including:
      * Slave mode and mode-fault error flags
      * Transmit and receive FIFO full and empty flags
* SPI Data Transmit Register
  + 0x[C\_BASEADDR + 68]
  + Write only
    - Data buffer register for AXI to SPI data
      * Tx\_FIFO input
      * Width controlled by generic C\_NUM\_TRANSFER\_BITS
* SPI Data Receive Register
  + 0x[C\_BASEADDR + 6C]
  + Read only
    - Data buffer register for SPI to AXI Data
      * Rx\_FIFO output
      * Width controlled by generic C\_NUM\_TRANSFER\_BITS
* SPI Slave Select Register
  + 0x[C\_BASEADDR + 70]
  + R/W
    - Active low, one hot encoded slave select vector
    - Slaves numbered right to left starting at zero with the LSB
* SPI Transmit FIFO Occupancy Register
  + 0x[C\_BASEADDR + 74]
  + Read only
    - Tx\_FIFO occupancy value
* SPI Receive FIFO Occupancy Register
  + 0x[C\_BASEADDR + 78]
  + Read only
    - Rx\_FIFO occupancy value
* Device Global Interrupt Enable Register
  + 0x[C\_BASEADDR + 1C]
  + R/W
    - Global enable allowing all enabled interrupts to pass to the interrupt controller
* IP Interrupt Status Register
  + 0x[C\_BASEADDR + 20]
  + R/W
    - Interrupt controls including:
      * Slave select mode, Slave mode-fault error, and mode fault error flags
        + Determines conflicts with mode configuration, slave select, and enable signals.
      * Data register/FIFO flags
        + Determines conflicts with data register/fifo occupancy and data read and write requests.
* IP Interrupt Enable Register
  + 0x[C\_BASEADDR + 28]
  + R/W
    - Individual interrupt enables